LISTING OF THE CLAIMS

IN THE CLAIMS:

Please cancel claims 1, 2, 6, 16 and 36-48; and

Please amend claim 3, 4, 7, 10, 14, 17, 28 and 31-34 as follows:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claims 1-2 (Canceled).

3. (Currently Amended) ~~The method of claim 2,~~ A method of manufacturing a structure, comprising the steps of:

providing a structure having an insulator layer with at least one interconnect;

forming a sub lithographic template mask over the insulator layer; and

selectively etching the insulator layer through the sub lithographic template mask to form sub lithographic features spanning to a sidewall of the at least one interconnect,

wherein the sub lithographic features are substantially vertical columns in the insulator layer, and

wherein the sub lithographic features further include a plurality of holes formed in a capping layer beneath the sub lithographic template mask and having a diameter or cross section less than a diameter or cross section of the at least one interconnect and also substantially equal to the substantially vertical columns in the insulator layer.

4. (Currently Amended) The method of claim [[1]] 3, wherein the etching step is an anisotropic etching forming a plurality of the sub lithographic features defined as nano columns.

5. (Original) The method of claim 4, wherein the etching step includes an isotropic etching to meld at least adjacent nano columns together and provide an undercut below the at least one interconnect.

Claim 6. (Canceled).

7. (Withdrawn – Currently Amended) The method of claim [[1]] 3, further comprising the step of depositing a capping layer prior to the forming step and pinching off a top portion of the capping layer to form pinched off structures having a sub lithographic diameter.

8. (Withdrawn) The method of claim 7, further comprising the step of depositing an insulating layer on the portion to form the pinched off structures.

9. (Withdrawn) The method of claim 8, wherein the depositing step forms insulator material on the sidewalls of the at least one interconnect, which was etched away during the etching step.

10. (Withdrawn – Currently Amended) The method of claim [[1]] 3, wherein the sub lithographic template mask is a diblock copolymer nanotemplate formed on a diffusion layer, the diffusion layer acting as a mask having features transferred from the diblock copolymer nanotemplate.

11. (Withdrawn) The method of claim 10, wherein the diblock copolymer nanotemplate has features smaller than spacings between adjacent interconnects.

12. (Withdrawn) The method of claim 10, wherein the diblock copolymer nanotemplate is a material which self assemblies itself into substantially uniformly shaped and spaced holes or features.

13. (Withdrawn) The method of claim 10, wherein the features of the diblock copolymer nanotemplate 150 are in a range from below 10 nm to 100 nm.

14. (Withdrawn – Currently Amended) The method of claim [[1]] 10, wherein the diblock copolymer nanotemplate is formed one of (i) partially over a blockout resist over the insulation layer and (ii) below the blockout resist, the blockout resist includes features that are larger than a spacing between adjacent interconnects.

15. (Withdrawn) The method of claim 14, further comprising the step of removing the block copolymer nanotemplate and blockout resist after the formation of the sub lithographic features in the insulation layer.

Claim 16 (Canceled).

17. (Withdrawn – Currently Amended) The method of claim [[1]] 3, wherein the sub lithographic template mask is a metal deposition layer which is treated to cause agglomeration.

18. (Withdrawn) The method of claim 17, wherein the metal deposition layer includes a material of one of Au, Ag, In, Sn and Ga.

19. (Withdrawn) The method of claim 17, wherein the agglomeration is formed by annealing and the agglomeration creates sub lithographic features in the range of 1 nm to 50 nm.

20. (Withdrawn) The method of claim 19, wherein the annealing causes nano islands which are used as a mask in an etching step.

21. (Withdrawn) The method of claim 17, wherein the metal deposition layer is deposited over a capping layer.

22. (Withdrawn) The method of claim 21, wherein the capping layer is formed from material from one of SiN, SiC and SiCOH

23. (Withdrawn) The method of claim 21, further comprising the steps of :

etching the capping layer though the sub lithographic features formed in the metal deposition layer to form pores corresponding to the features in the metal deposition layer;

removing the metal deposition layer; and

etching the insulation layer using the capping layer as a mask to form the sub lithographic features.

24. (Withdrawn) The method of claim 23, wherein the sub lithographic features are substantially vertical pores.

25. (Withdrawn) The method of claim 24, further comprising melding together adjacent vertical pores between the at least one interconnect.

26. (Withdrawn) The method of claim 23, wherein the sub lithographic features are backfilled with a second material than that of the insulation layer.

27. (Withdrawn) The method of claim 23, further comprising the step of providing a sealing cap over the sub lithographic features.

28. (Withdrawn – Currently Amended) The method of claim [[1]] 3, wherein the sub lithographic features are backfilled with a second material than that of the insulation layer.

29. (Withdrawn) The method of claim 27, wherein the sealing cap is selected from a material of SiN or SiC having a thickness in the range from 5 nm to 50 nm.

30. (Withdrawn) The method of claim 27, further comprising the step of depositing an insulator material on the sealing cap layer with a different characteristic.

31. (Withdrawn – Currently Amended) The method of claim [[1]] 3, wherein the sub lithographic template mask is formed from a random hole pattern in resist using e-beam, x-ray or EUV lithography.

32. (Withdrawn – Currently Amended) The method of claim [[1]] 3 wherein the sub lithographic template mask is a random hole pattern in a 2-phase polymer mask using a porogen

33. (Withdrawn – Currently Amended) The method of claim [[1]] 3, further comprising the step of forming a diblock patterning mask beneath the sub lithographic template mask.

34. (Withdrawn – Currently Amended) The method of claim [[1]] 3, further comprising providing a supra lithographic mask either over or underneath the sub lithographic template mask.

35. (Withdrawn) The method of claim 34, wherein the supra lithographic mask prevents formation of gaps over at least one area whose dimensions are larger than a minimum interconnect spacing.

Claims 36-57 (Canceled).